IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
COFLER)
)
Serial No. **Not Yet Assigned**)
)
Filing Date: **Herewith**)
)
FOR: METHOD OF HANDLING INSTRUCTIONS WITHIN A PROCESSOR WITH DECOUPLED ARCHITECTURE, IN PARTICULAR A PROCESSOR FOR DIGITAL SIGNAL PROCESSING, AND CORRESPONDING PROCESSOR)
)

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059949US

DATE OF DEPOSIT: February 26, 2002

NAME: Dawn Kimler

SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 24.

Please add new Claims 25 to 61.

25. A method for handling instructions within a processor with a decoupled architecture, the processor comprising a first processing unit including at least one register, first and second FIFO-type memories for storing

instructions for the second processing unit, the method comprising:

providing to the third FIFO-type memory an operative instruction for deriving an address of memory stored data;

providing to the first FIFO-type memory a loading instruction for loading the memory stored data into the at least one register, the loading instruction being executed only when the memory stored data has been delivered by the second processing unit, each loading instruction being provided to the first FIFO-type memory for storage therein and other operative instructions for the first processing unit being provided to the second FIFO-type memory for storage therein; and

removing from the second FIFO-type memory the operative instruction involving the at least one register after having reached an output of the second FIFO-type memory if no earlier loading instruction for modifying a value of the at least one register associated with this operative instruction is present in the first FIFO-type memory, and in the presence of such an earlier loading instruction, then removing the operative instruction from the second FIFO-type memory only after the loading instruction has been removed from the first FIFO-type memory.

26. A method according to Claim 25, wherein the first and second FIFO-type memories are separate from one another.

27. A method according to Claim 25, further

comprising:

storing a non-operative instruction in the first FIFO-type memory every time an operative instruction is stored in the second FIFO-type memory without provision being made simultaneously to store a loading instruction in the first FIFO-type memory;

incrementing a first read counter every time an instruction is removed from the first FIFO-type memory;

incrementing a first write counter every time an instruction is stored in the first FIFO-type memory;

storing a current value of the first write counter in a memory every time a loading instruction is stored in the first FIFO-type memory; and

comparing the current value of the first write counter with a current value of the first read counter for determining characteristics of the loading instruction in the first FIFO-type memory.

28. A method according to Claim 27, wherein a size of the first write and read counters are identical and equal to a size of the first FIFO-type memory; and further comprising:

changing a value of an overflow bit every time a respective first counter returns to its initial value;

storing a current value of the overflow bit of the first write counter in the memory every time a loading instruction is stored in the first FIFO-type memory; and

wherein comparing the current value of the first write counter with a current value of the first read counter

for determining characteristics of the loading instruction in the first FIFO-type memory further comprises comparing a current value of the overflow bit of the first read counter with the current value of the overflow bit of the first write counter.

29. A method according to Claim 28, further comprising:

associating a first label every time an operative instruction involving the at least one register is stored in the second FIFO-type memory, the first label containing the current value of the first write counter which was stored in the memory when a last loading instruction modifying the at least one register involved with the operative instruction was stored in the first FIFO-type memory; and

criteria for removing the stored operative instruction having reached an output of the second FIFO-type memory being based upon a result of a comparison between a current value associated with the stored operative instruction and the current value of the first read counter.

30. A method according to Claim 29, further comprising associating the current value of the overflow bit of the first write counter, which was stored in the memory when the last loading instruction modifying the at least one register involved with the operative instruction was stored in the first FIFO-type memory, with the operative instruction being stored in the second FIFO-type memory and its first label; and wherein the criteria for removing the stored

operative instruction having reached the output of the second FIFO-type memory also takes into account a result of the comparison between the current value associated with the stored operative instruction and the current value of the overflow bit of the first read counter.

31. A method according to Claim 25, wherein the processor further comprises fourth and fifth FIFO-type memories associated with the first processing unit, the fourth and fifth FIFO-type memories being separate from the first and second FIFO-type memories, and the first processing unit comprises a guard indication register; and further comprising:

providing a guarded instruction to the third FIFO-type memory or providing a guarded loading instruction to the first processing unit causes a transmission instruction to be provided to the first processing unit and stored in the fourth FIFO-type memory for causing transmission to the second processing unit or to the fifth FIFO-type memory, respectively, a value of a guard indication associated with the guarded instruction or with the guarded loading instruction, respectively;

if a modifying instruction earlier in time and intended to modify the value of the guard indication associated with the transmission instruction is not in the second FIFO-type memory, then removing the transmission instruction after having reached an output of the fourth FIFO-type memory; and

if the modifying instruction earlier in time and intended to modify the value of the guard indication

associated with the transmission instruction is in the second FIFO-type memory, then removing the transmission instruction from the fourth FIFO-type memory only after the modifying instruction has been removed from the second FIFO-type memory.

32. A method according to Claim 31, further comprising:

incrementing a second read counter every time an instruction is removed from the second FIFO-type memory;

incrementing a second write counter every time an instruction is stored in the second FIFO-type memory;

storing a current value of the second write counter in the memory every time a modifying instruction for modifying a value of a guard indication is stored in the second FIFO-type memory; and

comparing the stored current value of the second write counter with a current value of the second read counter for determining characteristics of the modifying instruction in the second FIFO-type memory.

33. A method according to Claim 32, wherein a size of the second write and read counters are identical and are equal to a size of the second FIFO-type memory; and further comprising:

changing a current value of an overflow bit every time a respective second counter returns to its initial value;

storing the current value of the overflow bit of the second write counter in a memory every time a modifying instruction is stored in the second FIFO-type memory; and

wherein comparing the stored current value of the second write counter with a current value of the second read counter for determining characteristics of the modifying instruction in the second FIFO-type memory further comprises comparing the current value of the overflow bit of the second read counter with the stored current value of the overflow bit of the second write counter.

34. A method according to Claim 33, further comprising:

associating a label with the transmission instruction being stored in the fourth FIFO-type memory, the label containing the current value of the second write counter which was stored in the memory when the last instruction modifying the guard indication associated with the transmission instruction was stored in the second FIFO-type memory; and

criteria for removing the transmission instruction after having reached an output of the fourth FIFO-type memory being based upon a result of the comparison between a current value of the stored transmission instruction and the current value of the second read counter.

35. A method according to Claim 34, further comprising:

associating the current value of the overflow bit of the second write counter, which was stored in the memory when the last modifying instruction modifying the guard

indication associated with the transmission instruction was stored in the second FIFO-type memory, with the transmission instruction being stored in the fourth FIFO-type memory and its label; and

criteria for removing this transmission instruction after having reached an output of the fourth FIFO-type memory also being based upon a result of the comparison between the stored current value associated with the transmission instruction and the current value of the overflow bit of the second read counter.

36. A method for handling instructions within a processor comprising a core including a plurality of processing units, and a plurality of FIFO-type memories for sequentially storing respective instructions for the plurality of processing units, the method comprising:

issuing an instruction within the core for loading memory stored data into at least one register of a first processing unit causes the core to

provide to a third FIFO-type memory, associated with a second processing unit, an operative instruction for deriving an address of the memory stored data,

provide to a first FIFO-type memory, associated with the first processing unit, a loading instruction for loading the memory stored data into the at least one register,

the loading instruction being executed when the memory stored data has been delivered by the second

processing unit, each loading instruction being provided to the first FIFO-type memory for storage therein and other operative instructions for the first processing unit being provided to the second FIFO-type memory for storage therein, and

removing from the second FIFO-type memory the operative instruction involving the at least one register after having reached an output of the second FIFO-type memory if no earlier loading instruction for modifying a value of the at least one register associated with this operative instruction is present in the first FIFO-type memory, and in the presence of such an earlier loading instruction, then removing the operative instruction from the second FIFO-type memory after the loading instruction has been removed from the first FIFO-type memory.

37. A method according to Claim 36, wherein the first and second FIFO-type memories are separate from one another.

38. A method according to Claim 36, further comprising:

storing a non-operative instruction in the first FIFO-type memory every time an operative instruction is stored in the second FIFO-type memory without provision being made simultaneously to store a loading instruction in the first FIFO-type memory;

incrementing a first read counter every time an instruction is removed from the first FIFO-type memory;

incrementing a first write counter every time an instruction is stored in the first FIFO-type memory;

storing a current value of the first write counter in a memory every time a loading instruction is stored in the first FIFO-type memory; and

comparing the current value of the first write counter with a current value of the first read counter for determining characteristics of the loading instruction in the first FIFO-type memory.

39. A method according to Claim 38, wherein a size of the first write and read counters are identical and equal to a size of the first FIFO-type memory; and further comprising:

changing a value of an overflow bit every time a respective first counter returns to its initial value;

storing a current value of the overflow bit of the first write counter in the memory every time a loading instruction is stored in the first FIFO-type memory; and

wherein comparing the current value of the first write counter with a current value of the first read counter for determining characteristics of the loading instruction in the first FIFO-type memory further comprises comparing a current value of the overflow bit of the first read counter with the current value of the overflow bit of the first write counter.

40. A method according to Claim 39, further comprising:

associating a first label every time an operative instruction involving the at least one register is stored in the second FIFO-type memory, the first label containing the current value of the first write counter which was stored in the memory when a last loading instruction modifying the at least one register involved with the operative instruction was stored in the first FIFO-type memory; and

criteria for removing the stored operative instruction having reached an output of the second FIFO-type memory being based upon a result of a comparison between a current value associated with the stored operative instruction and the current value of the first read counter.

41. A method according to Claim 40, further comprising associating the current value of the overflow bit of the first write counter, which was stored in the memory when the last loading instruction modifying the at least one register involved with the operative instruction was stored in the first FIFO-type memory, with the operative instruction being stored in the second FIFO-type memory and its first label; and wherein the criteria for removing the stored operative instruction having reached the output of the second FIFO-type memory also takes into account a result of the comparison between the current value associated with the stored operative instruction and the current value of the overflow bit of the first read counter.

42. A method according to Claim 36, wherein the processor further comprises fourth and fifth FIFO-type memories associated with the first processing unit, the fourth and fifth FIFO-type memories being separate from the first and second FIFO-type memories, and the first processing unit comprises a guard indication register; and further comprising:

providing a guarded instruction to the third FIFO-type memory or providing a guarded loading instruction to the first processing unit causes a transmission instruction to be provided to the first processing unit and stored in the fourth FIFO-type memory for causing transmission to the second processing unit or to the fifth FIFO-type memory, respectively, a value of a guard indication associated with the guarded instruction or with the guarded loading instruction, respectively;

if a modifying instruction earlier in time and intended to modify the value of the guard indication associated with the transmission instruction is not in the second FIFO-type memory, then removing the transmission instruction after having reached an output of the fourth FIFO-type memory; and

if the modifying instruction earlier in time and intended to modify the value of the guard indication associated with the transmission instruction is in the second FIFO-type memory, then removing the transmission instruction from the fourth FIFO-type memory only after the modifying instruction has been removed from the second FIFO-type memory.

43. A method according to Claim 42, further

comprising:

incrementing a second read counter every time an instruction is removed from the second FIFO-type memory;

incrementing a second write counter every time an instruction is stored in the second FIFO-type memory;

storing a current value of the second write counter in the memory every time a modifying instruction for modifying a value of a guard indication is stored in the second FIFO-type memory; and

comparing the stored current value of the second write counter with a current value of the second read counter for determining characteristics of the modifying instruction in the second FIFO-type memory.

44. A method according to Claim 43, wherein a size of the second write and read counters are identical and are equal to a size of the second FIFO-type memory; and further comprising:

changing a current value of an overflow bit every time a respective second counter returns to its initial value;

storing the current value of the overflow bit of the second write counter in a memory every time a modifying instruction is stored in the second FIFO-type memory; and

wherein comparing the stored current value of the second write counter with a current value of the second read counter for determining characteristics of the modifying instruction in the second FIFO-type memory further comprises

comparing the current value of the overflow bit of the second read counter with the stored current value of the overflow bit of the second write counter.

45. A method according to Claim 44, further comprising:

associating a label with the transmission instruction being stored in the fourth FIFO-type memory, the label containing the current value of the second write counter which was stored in the memory when the last instruction modifying the guard indication associated with the transmission instruction was stored in the second FIFO-type memory; and

criteria for removing the transmission instruction after having reached an output of the fourth FIFO-type memory being based upon a result of the comparison between a current value of the stored transmission instruction and the current value of the second read counter.

46. A method according to Claim 45, further comprising:

associating the current value of the overflow bit of the second write counter, which was stored in the memory when the last modifying instruction modifying the guard indication associated with the transmission instruction was stored in the second FIFO-type memory, with the transmission instruction being stored in the fourth FIFO-type memory and its label; and

criteria for removing this transmission instruction after having reached an output of the fourth FIFO-type memory also being based upon a result of the comparison between the stored current value associated with the transmission instruction and the current value of the overflow bit of the second read counter.

47. A processor comprising:

a first processing unit comprising at least one register;

first and second FIFO-type memories for storing instructions for said first processing unit;

a second processing unit;

a third FIFO-type memory for storing instructions for said second processing unit;

a central unit, in response to an instruction for loading memory stored data into said at least one register, providing to said third FIFO-type memory an operative instruction for deriving an address of the memory stored data, providing to said first FIFO-type memory a loading instruction for loading the memory stored data into said at least one register, the loading instruction being executed when the memory stored data has been delivered by said second processing unit, and providing each loading instruction to said first FIFO-type memory for storage therein and for providing other operative instructions for said first processing unit to said second FIFO-type memory for storage therein; and

a first controller for removing from said second FIFO-type memory an operative instruction involving said at least one register after having reached an output of said second FIFO-type memory if no earlier loading instruction for modifying a value of said at least one register associated with this operative instruction is present in said first FIFO-type memory, and in the presence of such an earlier loading instruction, then removing the operative instruction from said second FIFO-type memory after the loading instruction has been removed from said first FIFO-type memory.

48. A processor according to Claim 47, wherein said first and second FIFO-type memories are separate from one another.

49. A processor according to Claim 47, wherein said first controller comprises:

a first read counter incremented every time an instruction is removed from said first FIFO-type memory;

a first write counter incremented every time an instruction is stored in said first FIFO-type memory;

at least one first individual register associated with said at least one register;

a first control unit for storing a current value of said first write counter in a main field of said at least one first individual register associated said at least one register whenever a loading instruction for loading into said at least one register is stored in said first FIFO-type memory; and

a second control unit comprising a first comparison circuit for determining characteristics of the loading instruction in said first FIFO-type memory by comparing a content of the main field of said at least one first individual register with a current value of said first read counter.

50. A processor according to Claim 49, wherein a size of said first write and read counters are identical and are equal to a size of the first FIFO-type memory; wherein a value of an overflow bit changes value every time an associated first counter returns to its initial value; wherein each first individual register includes an auxiliary field; said first control unit stores a current value of the overflow bit of said first write counter in the auxiliary field of said at least one first individual register every time a loading instruction is loaded into said first FIFO-type memory; and said second control unit comprises a first auxiliary comparison circuit for comparing a current value of the overflow bit of said first read counter with a content of the auxiliary field.

51. A processor according to Claim 50, wherein said first auxiliary comparison circuit comprises an exclusive NOR logic gate.

52. A processor according to Claim 50, wherein said second FIFO-type memory comprises a plurality of stages including an input stage and an output stage, and a useable

field for storing at least one operative instruction involving said at least one register, and a second supplementary field; and wherein said at least one register comprises a plurality of registers, and said at least one first individual register comprises a plurality of first individual registers; and further comprising:

a third control unit able, every time an operative instruction involving at least one of said plurality of registers is stored in the usable field of the input stage of said second FIFO-type memory, to select from among all said plurality of first individual registers associated with all of said plurality of registers involved in the operative instruction, the one corresponding to a last loading instruction for modifying at least one of said plurality of registers involved, and for transferring a content of the main field of a selected first individual register, into the first supplementary field of the input stage of said second FIFO-type memory; and

a fourth control unit comprising a first comparison circuit for deriving criteria for removing the operative instruction after having reached the output stage of said second FIFO-type memory by comparing a content of the first supplementary field of the output stage with the current value of said first read counter.

53. A processor according to Claim 52, wherein each stage of said second FIFO-type memory further includes a second supplementary field; said third control unit being able, every time an operative instruction is stored in the

usable field of the input stage of the second FIFO-type memory, for transferring a content of the auxiliary field of a selected first individual register, into the second supplementary field of the input stage of said second FIFO-type memory; and said fourth control unit comprises a first supplementary comparison circuit for comparing a content of the second supplementary field with the current value of the overflow bit of said first read counter.

54. A processor according to Claim 53, wherein said first supplementary comparison circuit comprises an exclusive NOR logic gate.

55. A processor according to Claim 47, further comprising fourth and fifth FIFO-type memories associated with said first processing unit, said fourth and fifth FIFO-type memories being separate from said first and second FIFO-type memories; wherein said first processing unit comprises a guard indication register; said central unit providing a guarded instruction to said third FIFO-type memory or providing a guarded loading instruction to said first processing unit causes a transmission instruction to be provided to said first processing unit and stored in said fourth FIFO-type memory for causing transmission to said second processing unit or to said fifth FIFO-type memory, respectively, a value of a guard indication associated with the guarded instruction or with the guarded loading instruction, respectively; and further comprising a second controller for removing the transmission instruction from said fourth FIFO-type memory after the

modifying instruction has been removed from said second FIFO-type memory if the modifying instruction earlier in time and intended to modify the value of the guard indication associated with the transmission instruction is not in said second FIFO-type memory, and if the modifying instruction earlier in time and intended to modify the value of the guard indication associated with the transmission instruction is in said second FIFO-type memory, then removing the transmission instruction from said fourth FIFO-type memory after the modifying instruction has been removed from the second FIFO-type memory.

56. A processor according to Claim 55, wherein said second controller comprises:

a second read counter incremented every time an instruction is removed from said second FIFO-type memory;

a second write counter incremented every time an instruction is stored in said second FIFO-type memory;

a plurality of second individual registers associated respectively with a plurality of guard indications;

a fifth control unit able, every time a modifying instruction for modifying a value of a guard indication is stored in said second FIFO-type memory, to store the current value of the second write counter in a main field of one of said plurality of second individual registers associated with the guard indication; and

a sixth control unit comprising a second comparison circuit for determining characteristics of the modifying instruction in said second FIFO-type memory by comparing a

content of the main field of one of said plurality of second individual registers a current value of said second read counter.

57. A processor according to Claim 56, wherein a size of said second write and read counters are identical and equal to a size of said second FIFO-type memory; and an overflow bit that changes value every time a corresponding second counter returns to its initial value is associated with each second counter; each second individual register further includes an auxiliary field; said fifth control unit is able, every time a modifying instruction modifying a value of a guard indication is stored in said second FIFO-type memory, to store the current value of the overflow bit of said second write counter in the auxiliary field of said corresponding second individual register; and said sixth control unit comprises a second auxiliary comparison circuit for comparing a current value of the overflow bit of said second read counter with a content of the auxiliary field.

58. A processor according to Claim 57, wherein said second auxiliary comparison circuit comprises an exclusive NOR logic gate.

59. A processor according to Claim 57, wherein each stage of said fourth FIFO-type memory includes a usable field for storing a transmission instruction, and a first supplementary field; said second controller comprising:

a seventh control unit able, every time a transmission instruction is stored in the usable field of the input stage of said third FIFO-type memory, to transfer a content of the main field of said plurality of second individual registers associated with the corresponding guard indication into the first supplementary field of the input stage of said fourth FIFO-type memory; and

an eighth control unit for determining criteria for removing the transmission instruction having reached an output stage of said fourth FIFO-type memory, and comprising a second comparison circuit for comparing a content of the first supplementary field of the output stage with the current value of said second read counter.

60. A processor according to Claim 59, wherein each stage of said fourth FIFO-type memory further includes a second supplementary field; said seventh control unit is able, every time a transmission instruction is stored in the usable field of the input stage of said fourth FIFO-type memory, to transfer a content of the auxiliary field of said second individual register associated with the corresponding guard indication into the second supplementary field of the input stage of said third FIFO-type memory; said eighth control unit comprises a second supplementary comparison circuit for comparing a content of the second supplementary field with the current value of the overflow bit of said second read counter.

61. A processor according to Claim 60, wherein said

second supplementary comparison circuit comprises an exclusive NOR logic gate.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner=s convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

MICHAEL W. TAYLOR
Reg. No. 43,182
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorneys for Applicant